Chapter 6
PROBLEMS

1. [E, None, 4.2] Implement the equation \( X = ((\overline{A} + \overline{B}) (\overline{C} + \overline{D} + \overline{E}) + \overline{F}) \overline{G} \) using complementary CMOS. Size the devices so that the output resistance is the same as that of an inverter with an NMOS \( W/L = 2 \) and PMOS \( W/L = 6 \). Which input pattern(s) would give the worst and best equivalent pull-up or pull-down resistance?

**Solution**

Rewriting the output expression in the form \( X = ((\overline{A} + \overline{B}) (\overline{C} + \overline{D} + \overline{E}) + \overline{F}) \overline{G} = ((AB + CDE)F) + G \) allows us to build the pulldown network by inspection (parallel devices implement an OR, and series devices implement an AND). The pullup network is the dual of the pulldown network.

![Diagram of CMOS implementation](attachment:image.png)

The plot shows sizes that meet the requirement - in the worst case, the output resistance of the circuit matches the output resistance of an inverter with NMOS \( W/L = 2 \) and PMOS \( W/L = 6 \).

The worst case pull-up resistance occurs whenever a single path exists from the output node to \( Vdd \). Examples of vectors for the worst case are \( ABCDEFG=1111100 \) and \( 0101110 \). The best case pull-up resistance occurs when \( ABCDEFG=0000000 \).

The worst case pull-down resistance occurs whenever a single path exists from the output node to \( GND \). Examples of vectors for the worst case are \( ABCDEFG=0000001 \) and \( 0011110 \).

The best case pull-down resistance occurs when \( ABCDEFG=1111111 \).

2. Implement the following expression in a full static CMOS logic fashion using no more than 10 transistors:

\[ F = (A \cdot B) + (A \cdot C \cdot E) + (D \cdot E) + (D \cdot C \cdot B) \]

**Solution**
3. Consider the circuit of Figure 6.1.

The logic function is: $Y = (A + B)CD$. The transistor sizes are given in the figure above.

b. What are the input patterns that give the worst case $t_{phl}$ and $t_{plh}$? State clearly what are the initial input patterns and which input(s) has to make a transition in order to achieve this maximum propagation delay. Consider the effect of the capacitances at the internal nodes.

Solution

The worst case $t_{phl}$ happens when the internal node capacitances ($C_{x2}$ and $C_{x3}$) are charged before the high to low transition. The initial states that can cause this are: ABCD=[1010, 1110, 0110]. The final state is one of: ABCD=[1011, 0111].
The worst case \( t_{\text{PHL}} \) happens when \( Cx1 \) is charged before the low to high transition. The input pattern that can cause this is: \( ABCD = [0111] \Rightarrow [0011] \).

c. Verify part (b) with SPICE. Assume all transistors have minimum gate length (0.25 \( \mu \text{m} \)).

**Solution**

The two cases are shown below.

\[ \text{Figure 6.2 Best and worst } t_{\text{PHL}}. \]

\[ \text{Figure 6.3 Best and worst } t_{\text{PLH}}. \]

d. If \( P(A=1)=0.5, P(B=1)=0.2, P(C=1)=0.3 \) and \( P(D=1)=1 \), determine the power dissipation in the logic gate. Assume \( V_{DD}=2.5 \text{V}, C_{out}=30 \text{fF} \) and \( f_{clk}=250 \text{MHz} \).

**Solution**

Since \( D \) is always 1, the circuit implements the following function
\[ Y = (A + B)C. \]

\( P_{(A+B)=1} = P_{A=0}P_B = 0.5 \times (1-0.2) = 0.4, \)

\( P_{(A+B)=0} = 1 - 0.4 = 0.6, \)

\( P_Y = 0 = P_{(A+B)=1}P_C = 1 = 0.6 \times 0.3 = 0.18 \)

\( P_Y = 1 = 1 - 0.18 = 0.82 \)

\( P_{Y=0 \Rightarrow 1} = 0.18 \times 0.82 = 0.1476 \)

So \( P_{\text{dyn}} = P_{Y=0 \Rightarrow 1}C_{out}V_{DD}^2f_{clk} = (0.1476)(30 \times 10^{-15})(2.5^2)(250 \times 10^6) = 6.92 \mu \text{W}. \)

4. [M. None, 4.2] CMOS Logic

a. Do the following two circuits (Figure 6.4) implement the same logic function? If yes, what is that logic function? If no, give Boolean expressions for both circuits.
Yes, they implement the same logic function:
\[ F = (ABCD + E) = (A + B + C + D).E \]

b. Will these two circuits’ output resistances always be equal to each other?

Solution

No

c. Will these two circuits’ rise and fall times always be equal to each other? Why or why not?

Solution

No. Circuit B appears optimized for the case where the transistor with input E is on the critical path since it is closer to the output node than in circuit A. Therefore, if input E arrives later, circuit B will be faster than circuit A since the internal node will already be charged and only the output capacitance needs to be switched. Even if we assume, all inputs arrive at the same time, however, the two circuits rise and fall times will not be equal to each other. Consider an input combination where E,A,B,C,D are all low. Circuit A has only one body-affected device while circuit B has four. Since the associated rise in \( V_t \) and fall in output resistance affects only one resistor in circuit A, but four parallel resistors in circuit B, we expect a difference in the timing waveforms.

![Figure 6.4 Two static CMOS gates.](image)

5. [E, None, 4.2] The transistors in the circuits of the preceding problem have been sized to give an output resistance of 13 k\( \Omega \) for the worst-case input pattern. This output resistance can vary, however, if other patterns are applied.

a. What input patterns (A–E) give the lowest output resistance when the output is low? What is the value of that resistance?

Solution

The lowest output resistance is obtained when all inputs (A, B, C, D and E) are equal to 1. In that case, the output resistance is the parallel of the resistance of a nMOS of width 1, with a series of four equal nMOS of width 4. Both combinations have the same resistance, equal to the worst-case output resistance, 13 k\( \Omega \). Then the output resistance, in this case, is half this value, 6.5 k\( \Omega \).

b. What input patterns (A–E) give the lowest output resistance when the output is high? What is the value of that resistance?
Solution

The lowest output resistance is obtained when all inputs are equal to zero. Each of the pMOS have the same width, so all of them have the same resistance. The worst case resistance happens when only one of the inputs (A, B, C or D) is equal to 0 while all the rest are equal to 1. The output resistance in that case is the series of the resistance of two of the pMOS and it is equal to 13 kΩ. Then, each of the pMOS has an output resistance equal to 6.5 kΩ. The output resistance is equal to the series of one of these resistances with the parallel of four of the same resistances. Then, the minimum output resistance is 6.5 kΩ + 6.5 kΩ /4 = 8.125 kΩ.

6. [E, None, 4.2] What is the logic function of circuits A and B in Figure 6.5? Which one is a dual network and which one is not? Is the nondual network still a valid static logic gate? Explain. List any advantages of one configuration over the other.

![Figure 6.5 Two logic functions.](image)

Solution

Both circuits A and B implement the XOR logic function. Circuit A is a dual network because the pull up network is dual with the pull down network.

However, circuit B is still a valid static logic gate, because for any combination of the inputs, there is either a low resistance path from $V_{DD}$ or ground to the output. Circuit B has an extra advantage. The internal node capacitances are less compared to Circuit A, which make it faster than Circuit A.

7. [E, None, 4.2] Compute the following for the pseudo-NMOS inverter shown in Figure 6.6:

a. $V_{OL}$ and $V_{OH}$

Solution

To find $V_{OH}$, set $V_{in}$ to 0, because $V_{OL}$ is likely to be below $V_{DD}$ for the NMOS. If $V_{in}$=0, then $M_1$ is off, so the PMOS pulls the output all the way to the rail. So, $V_{OH}=V_{DD}=2.5V$.

To find $V_{OL}$, set $V_{in}$ = $V_{OH}$ = 2.5V. The NMOS is all the way on, but so is the PMOS. To find $V_{OL}$, we can write a current balancing equation at the output node: $I_{on} + I_{off} = 0$. First, we must determine the region of operation for each device. We can assume that $V_{DS} = V_{OL}$ for the NMOS is less than $V_{DSAT}$, so the NMOS is in the linear region. $V_{DS}$ for the PMOS will be more negative than $V_{DSAT}$, and $V_{GS} = -2.1$, so the PMOS is velocity saturated. The equation is therefore:

$$k' \frac{W}{L} V_{DSAT} \cdot (V_{GT} - 0.5V_{DSAT}) \cdot (1 + \lambda V_{DS}) + k' \frac{W}{L} V_o \cdot (V_{GT} - 0.5V_o) \cdot (1 + \lambda V_o) = 0$$

Plugging in numbers (process parameters such as $V_{DSAT}$ appear in tables in previous chapters) gives:
Solving for $V_o$ gives $V_{OL} = 31.6\text{mV}$.

b. $NM_L$ and $NM_H$

**Solution**

Rather than calculating the derivative of the current, we will estimate $V_{IL}$ and $V_{IH}$ from the simulated VTC. This approach estimates that the noise margin low is about 0.47V and the noise margin high is about 1.67V.

c. The power dissipation: (1) for $V_{in}$ low, and (2) for $V_{in}$ high

**Solution**

For $V_{in}$ low, the NMOS is off, so the power dissipation is 0W. For $V_{in}$ high, $P=V\cdot I_{DP}$. We saw in part a) the equation for $I_{DP}$. Plugging in the value for $V_{OL}$, we get $P=1.25\cdot120\mu\text{A} = 30\mu\text{W}$.

d. For an output load of 1 pF, calculate $t_{pLH}$, $t_{pHL}$, and $t_p$. Are the rising and falling delays equal? Why or why not?

**Solution**

We cannot use the estimate of resistance from the I-V curve for the HL transition because the PMOS is still on. Therefore, we will use the average current method for estimating delay. The average current for the HL transition through the PMOS is $0.5(I_{VDD=2.5} + I_{VDD=1.25})$. $I_{VDD=2.5} = 0$. $I_{VDD=1.25} = -30(2)(-1.6)\cdot(1-0.1(2.5)) = 108\mu\text{A}$. Thus, $I_{avg}$ for the PMOS is 54uA.

For the NMOS, $I_{VDD=2.5} = 115(16)(2.07-0.5)(1+0.06+2.5) = 2.4\text{mA}$ and $I_{VDD=1.25} = 115(16) (0.63) (2.07-0.5)(1+0.06+1.25) = 2.2\text{mA}$. So, $I_{avg}$ for the NMOS is 2.3mA. The average current discharging the capacitor is then $2.3\text{mA}-54\mu\text{A} = 2.25\text{mA}$. Then $t_{PLH} = C\tau_{VDD}/I_{avg} = 556\text{ps}$.

For $t_{pLH}$, the NMOS is off, so we can use equivalent resistance to find the transition time. From the table of resistances in the text, we can calculate $R_{eq} = 31\Omega/(W/L) = 15.5\Omega$. Then $t_{pLH} = 0.69\times R_{eq}$ So $t_{pLH} = 10.7\text{ns}$.

$t_p = (t_{pLH} + t_{pHL})/2 = 5.6\text{ns}$. The rising delay is much longer because the PMOS is very weak relative to the NMOS.

8. [M, SPICE, 4.2] Consider the circuit of Figure 6.7.

a. What is the output voltage if only one input is high? If all four inputs are high?

**Solution**

\[ -30 \cdot 2 \cdot -1 \cdot (1.6) \cdot (1 - 0.1(V_o - 2.5)) + 115(16) \cdot V_o \cdot (2.07 - 0.5V_o) \cdot (1 + 0.06V_o) = 0 \]

The output voltage is $V_o = 2.5 \text{V}$.
Consider a case when one input is high: \( A = V_{DD} \) and \( B = C = D = 0 \, V \). Assume that \( V_{out} \) is small enough that \( V_{min} = V_{DSAT} \) for the PMOS device, and \( V_{min} = V_{DS} = V_{out} \) for the NMOS devices. Solve for \( V_{out} \) by setting the drain currents in the PMOS and NMOS equal to each other, \( |I_{DP}| = |I_{DN}| \), where the drain currents are functions of \( V_{out}, V_{DD} \), and the device parameters.

\( V_{out} = 102 \, mV, \) and \( I_{D} = 35.7 \, \mu A. \)

Now verify that the assumptions for \( V_{min} \) are correct. For the PMOS: \( V_{DS} = -2.34 \, V, \) \( V_{DSAT} = -1 \, V, \) \( V_{GT} = -2.1 \, V, \) therefore \( V_{min} = V_{DSAT} \). For the NMOS: \( V_{DS} = 102 \, mV, \) \( V_{DSAT} = 630 \, mV, \) \( V_{GT} = 2.07 \, V, \) therefore \( V_{min} = V_{DS}. \)

Consider the case when all inputs are high: \( A = B = C = D = V_{DD} \). For these hand calculations, this is numerically equivalent to a circuit with a single NMOS device with \( W/L = 4 \times 1.5 \) and its gate tied to \( V_{DD} \). Now, the analysis used above for the case when one device is on can be reused, replacing \( W/L \) of the NMOS with 6, and using the same assumptions for \( V_{min}. \) \( V_{out} = 25 \, mV, \) and \( I_{D} = 35.9 \, \mu A. \) The assumptions for \( V_{min} \) are correct.

b. What is the average static power consumption if, at any time, each input turns on with an (independent) probability of 0.5? 0.1?

**Solution**

Notice in part a) that the drain current in the PMOS is 35.7 \( \mu A \) with one NMOS on and 35.9 \( \mu A \) with four NMOS devices on. The current in the PMOS can be approximated as 35.8 \( \mu A \) when any number of NMOS devices are on and 0 \( \mu A \) when all four are off. The probability that all four NMOS devices are off is \( (1 - \rho)^4 \) where \( \rho \) is the probability an input is high. Therefore,

\[
P_{AVG} = P_{OFF} \cdot (1 - \rho)^4 + P_{ON} \cdot [1 - (1 - \rho)^4]
\]

where \( P_{OFF} = 0 \, \text{W}, \) and \( P_{ON} = 89.5 \, \mu W. \) \( P_{AVG} = 83.9 \, \mu W \) when \( \rho = 0.5 \) and \( P_{AVG} = 30.7 \, \mu W \) when \( \rho = 0.5. \)

c. Compare your analytically obtained results to a SPICE simulation.

**Solution**

From SPICE: \( V_{out} = 98.7 \, mV, \) and \( I_{D} = 38.2 \, \mu A \) with one NMOS device on and \( V_{out} = 23.5 \, mV, \) and \( I_{D} = 38.3 \, \mu A \) with all NMOS devices on.

![Figure 6.7 Pseudo-NMOS gate.](image)

9. [M, None, 4.2] Implement \( F = ABC + \overline{A}CD \) (and \( \overline{F} \)) in DCVSL. Assume \( A, B, C, D, \) and their complements are available as inputs. Use the minimum number of transistors.
10. [E, Layout, 4.2] A complex logic gate is shown in Figure 6.8.
   a. Write the Boolean equations for outputs $F$ and $G$. What function does this circuit implement?

   **Solution**
   
   $G = A(XOR)B$
   $F = A(XNOR)B$

   b. What logic family does this circuit belong to?

   **Solution**
   
   It belongs to the DCVSL logic family.

   c. Assuming $W/L = 0.5\mu/0.25\mu$ for all nmos transistors and $W/L = 2\mu/0.25\mu$ for the pmos transistors, produce a layout of the gate using Magic. Your layout should conform to the following datapath style: (1) Inputs should enter the layout from the left in polysilicon; (2) The outputs should exit the layout at the right in polysilicon (since the outputs would probably be driving transistor gate inputs of the next cell to the right); (3) Power and ground lines should run vertically in metal 1.

   **Figure 6.8** Two-input complex logic gate.

   d. Extract and netlist the layout. Load both outputs (F,G) with a 30fF capacitance and simulate the circuit. Does the gate function properly? If not, explain why and resize the transistors so that it does. Change the sizes (and areas and perimeters) in the HSPICE netlist.

   **Solution**
   
   The gate doesn’t function properly, because the PMOS devices are strong and the NMOS pull down network can not switch the output nodes.
If you decrease the PMOS sizes to W=0.5 \text{um}, then the logic gate will function properly.

11. Design and simulate a circuit that generates an optimal differential signal as shown in Figure 6.9. Make sure the rise and fall times are equal.

\[
\begin{array}{c|c|c}
A & Y & \overline{Y} \\
0 & 0 & 1 \\
1 & 1 & 0 \\
\end{array}
\]

\textbf{Figure 6.9} Differential Buffer.

\textbf{Solution}

The circuit is shown below.

\textbf{If the inverters are sized for equal rise and fall times then you can achieve equal rise and fall times on the differential outputs, as long as the other FETs are sized symmetrically.}

12. What is the function of the circuit in Figure 6.10?

\textbf{Solution}

The circuit implements an S-R latch. Set is A and Reset is B. The invalid state is when both A and B are 0.

13. Implement the function \( S = ABC + \overline{ABC}C + \overline{AB}C + \overline{A}BC \), which gives the sum of two inputs with a carry bit, using NMOS pass transistor logic. Design a DCVSL gate which implements the same function. Assume \( A, B, C \), and their complements are available as inputs.

\textbf{Solution}
The two cases are shown in the figure below.

14. Describe the logic function computed by the circuit in Figure 6.11. Note that all transistors (except for the middle inverters) are NMOS. Size and simulate the circuit so that it achieves a 100 ps delay (50-50) using 0.25μm devices, while driving a 100 fF load on both differential outputs. ($V_{DD} = 2.5V$). Assume $A$, $B$ and their complements are available as inputs.

Figure 6.11 Cascoded Logic Styles.
For the drain and source perimeters and areas you can use the following approximations: \( A_S = A_D = W \times 0.625 \mu \) and \( A_P = A_D = W + 1.25 \mu \).

15. **Solution**
   The circuit implements an XOR. The sizes of the transistors are \( M_1: 28 \mu/0.25 \mu, M_2: 28 \mu/0.25 \mu, M_3: 10 \mu/0.25 \mu, M_4: 10 \mu/0.25 \mu, M_{P_{inv}}: 4 \mu/0.25, M_{N_{inv}}: 0.375 \mu/10 \mu \)

16. **Solution**
   - Determine the truth table for the circuit. What logic function does it implement?
     - The truth table is shown below
     
     | AB  | Out |
     |-----|-----|
     | 00  | 1   |
     | 01  | 0   |
     | 10  | 0   |
     | 11  | 1   |

   The circuit implements an XNOR.
   - Assuming 0 and 2.5 V inputs, size the PMOS transistor to achieve a \( V_{OL} = 0.3 \) V.
     - Solution
       The PMOS device will be velocity saturated and the NMOS passgate will be in the linear region. \( I_{DN} + I_{DP} = 0 \), so
       
       \[
       k'_{p} \frac{W}{L} V_{DSAT} \cdot (V_{GT} - 0.5V_{DSAT}) \cdot (1 + \lambda V_{DS}) + k'_{n} \frac{W}{L} V_{DS} \cdot (V_{GT} - 0.5V_{DS}) \cdot (1 + \lambda V_{DS}) = 0
       \]

       We know that \( V_{DS} = 0.3 \) V, so we can plug in numbers and solve for \( W/L \) for the PMOS is 7. Let the PMOS be \( 1.75/0.25 \).
   - If the PMOS were removed, would the circuit still function correctly? Does the PMOS transistor serve any useful purpose?
     - Solution
       No. If the PMOS were removed, the output node could remain low when \( AB = 00 \) because it would be floating. The PMOS device pulls the output node high when it would otherwise be in a high impedance state.

17. **Solution**
   This problem considers the effects of process scaling on pass-gate logic.
a. If a process has a $t_{buf}$ of 0.4 ns, $R_{eq}$ of 8 kΩ, and $C$ of 12 fF, what is the optimal number of stages between buffers in a pass-gate chain?

**Solution**

$$m_{opt} = 1.7 \sqrt{t_{buf} / (R_{eq} \cdot C)} = 3.47 \approx 3 \text{ gates between buffers.}$$

b. Suppose that, if the dimension of this process are shrunk by a factor $S$, $R_{eq}$ scales as $1 / S^2$, $C$ scales as $1 / S$, and $t_{buf}$ scales as $1 / S^2$. What is the expression for the optimal number of buffers as a function of $S$? What is this value if $S = 2$?

**Solution**

$$m_{opt} = 1.7 \sqrt{t_{buf} / (R_{eq} \cdot C)} = 4.9 \approx 5 \text{ gates between buffers.}$$

18. [C, None, 4.2] Consider the circuit of Figure 6.13. Let $C_x = 50 \text{ fF}$, $M_r$ has $W/L = 0.375/0.375$, $M_n$ has $W/L_{eff} = 0.375/0.25$. Assume the output inverter doesn’t switch until its input equals $V_{DD}/2$.

a. How long will it take $M_n$ to pull down node $x$ from 2.5 V to 1.25 V if $I_{in}$ is at 0 V and $B$ is at 2.5 V?

**Solution**

To determine the time required for these transitions, we will find the average currents in the FETs $M_r$ and $M_n$. The equivalent resistance method will not suffice since it does not account for both devices being on.

For $M_r$, $I_{VDD=2.5}$ = 0 since $V_{DS} = 0$. For the other case, the PMOS device is velocity saturated, so:

$$I_{VDD=1.25} = (30)(1)(1.5)(0.63)(2.07-0.63/2)(1+0.06*2.5) = -54 \mu A.$$ The average current in the PMOS is -27 $\mu A$.

$M_n$ is in the velocity saturation region for both endpoints of the transition. The two currents are therefore:

$$I_{VDD=2.5} = (115)(1.5)(0.63)(2.07-0.63/2)(1+0.06*2.5) = 219 \mu A.$$ $I_{VDD=1.25} = (115)(1.5)(0.63)(2.07-0.63/2)(1+0.06*2.5) = 205 \mu A.$

And the average current in the NMOS is 212 $\mu A$.

The total current DISCHARGING the capacitor is 211 $\mu A - 27 \mu A = 185 \mu A$.

The time for the transition is then

$$t = \frac{C \cdot \Delta V}{I_{avg}} = \frac{50 \text{ fF} \cdot 1.25 \text{ V}}{185 \mu A} = 338 \text{ ps}.$$  

b. How long will it take $M_n$ to pull up node $x$ from 0 V to 1.25 V if $I_{in}$ is 2.5 V and $B$ is 2.5 V?

**Solution**

For the LH transition, the PMOS “keeper” is off. The NMOS $M_n$ is the only FET that is on for this transition. We present both methods for finding the pull-up time.

**Equivalent Resistance:** We need to perform a different sweep for this measurement than the regular $I_D$ vs $V_{DS}$ sweep. In this case, $V_{DS}$ is changing because the source node of the FET is rising. Since the source voltage is changing, $V_{GS}$ also is reducing as node $x$ rises. This effectively “turns down” the current the NMOS can sustain. Performing the appropriate sweep and measuring $R_{eq}$ gives $R_{eq} = (11.3k \Omega + 34.7k \Omega) / 2 = 23k \Omega$. Thus, $t = 0.69*C*R_{eq} = 0.69*50 \text{ fF}*23k \Omega = 794 \text{ ps}$.

**Average Current:** When $x = 0$, the pass transistor has a $V_{GS} = 2.5$ and a $V_{DS} = 2.5$, so it is velocity saturated.

$$I_{x=0} = (115)(1.5)(0.63)(2.07-0.63/2)(1+0.06*2.5) = 219 \mu A.$$
When \( x = 1.25 \), the pass transistor has \( V_{DS} = 1.25 \) and \( V_{GS} = 1.25 \). It is still velocity saturated, but notice that \( V_{GS} \) has decreased. Thus,

\[
I_{x=1.25} = (115)(1.5)(0.63)(1.25-0.43-0.63/2)(1+0.06*1.25) = 59\mu A.
\]

The average current is then \( I_{avg} = 139\mu A \).

\[
t = \frac{C \cdot \Delta V}{I_{avg}} = \frac{50fF \cdot 1.25V}{139\mu A} = 450\text{ps}.
\]

Clearly, the two solutions are not very close together. The actual simulated transition time is about 644ps. The \( I_{avg} \) approximation underestimates the solution because the true average current in this case is not close to the average of the endpoints. In a typical inverter (PMOS pullup and NMOS pulldown), \( V_{GS} \) doesn’t change over the transition, so the current is reasonably linear with \( V_{DS} \). For that case, the average current is close to the average of the endpoints. In this problem, the pinch-off of \( V_{GS} \) in the pass transistor means the average is closer to the smaller value. Numerical calculation of the average current from an HSPICE sim gives \( I_{avg} = 93\mu A \) which would give a transition time of \( t = 672\text{ps} \), which is much closer to the actual value.

c. What is the minimum value of \( V_B \) necessary to pull down \( V_x \) to 1.25V when \( V_{in} = 0 \) V?

**Solution**

In order for \( M_n \) to pull node \( x \) low, the current in \( M_n \) must equal or exceed the current that charges up the capacitor at every point in the transition. The maximum current in \( M_n \) occurs when \( x = 1.25 \) V, and it is (from part a) \( I_{M_n} = -54\mu A \). We can write a current equation for \( M_n \) at this point in the transition and solve for \( V_B \):

Note that \( M_n \) is velocity saturated at this point: \( 54 = 115(1.5)(0.63)(V_B-0.43-0.63/2)(1+0.06*1.25) \).

Solving gives \( V_B = 1.207V \).

![Figure 6.13 Level restorer.](image-url)
19. Pass Transistor Logic

Consider the circuit of Figure 6.14. Assume the inverter switches ideally at $V_{DD}/2$, neglect body effect, channel length modulation and all parasitic capacitance throughout this problem.

a. What is the logic function performed by this circuit?

**Solution**

The circuit is a NAND gate.

b. Explain why this circuit has non-zero static dissipation.

**Solution**

When $A=B=V_{DD}$, the voltage at node $x$ is $V_x=V_{DD}-V_{tN}$. This causes static power dissipation at the inverter the pass transistor network is driving.

c. Using only just 1 transistor, design a fix so that there will not be any static power dissipation. Explain how you chose the size of the transistor.

**Solution**

The modified circuit is shown in the next figure.

![Circuit Diagram](image)

The size of $M_r$ should be chosen so that when one of the inputs $A$ or $B$ equals 0, either $M_{n1}$ or $M_{n2}$ would be able to pull node $X$ to $V_{DD}/2$ or less.

d. Implement the same circuit using transmission gates.

**Solution**

![Circuit Diagram](image)
The circuit is shown below.

**e.** Replace the pass-transistor network in Figure 6.14 with a pass transistor network that computes the following function: \( x = ABC \) at the node \( x \). Assume you have the true and complementary versions of the three inputs \( A, B \) and \( C \).

**Solution**

One possible implementation is shown.

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20. [M, None, 4.3] Sketch the waveforms at \( x, y, \) and \( z \) for the given inputs (Figure 6.15). You may approximate the time scale, but be sure to compute the voltage levels. Assume that \( V_T = 0.5 \) V when body effect is a factor.

21. [E, None, 4.3] Consider the circuit of Figure 6.16.

**a.** Give the logic function of \( x \) and \( y \) in terms of \( A, B, \) and \( C \). Sketch the waveforms at \( x \) and \( y \) for the given inputs. Do \( x \) and \( y \) evaluate to the values you expected from their logic functions? Explain.

**Solution**

\[ x = \overline{AB} \text{ and } y = ABC \]

The circuit does not correctly implement the desired logic function. This stems from the fact that \( x \) is pre-charged high, and thus node \( y \) is discharged as soon as the evaluation phase starts. Although \( x \) is eventually discharged by the first stage, \( y \) cannot be charged high again since it is a dynamic node with no low-impedance path to Vdd (during evaluate). Common solutions to this problem are to either place an inverter between the two stages (thus allowing only 0-to-1 transitions on the inputs to each stage during evaluate) as in Domino logic or employing np-CMOS. The latter is presented in (b).

**b.** Redesign the gates using np-CMOS to eliminate any race conditions. Sketch the waveforms at \( x \) and \( y \) for your new circuit.

**Solution**
22. [M. None, 4.3] Suppose we wish to implement the two logic functions given by $F = A + B + C$ and $G = A + B + C + D$. Assume both true and complementary signals are available.

a. Implement these functions in dynamic CMOS as cascaded $\phi$ stages so as to minimize the total transistor count.

**Solution**

Dynamic gates with NMOS pull-down networks cannot be directly cascaded. This solution uses a domino logic approach.

b. Design an $np$-CMOS implementation of the same logic functions.

**Solution**
23. Consider a conventional 4-stage Domino logic circuit as shown in Figure 6.17 in which all precharge and evaluate devices are clocked using a common clock $\phi$. For this entire problem, assume that the pulldown network is simply a single NMOS device, so that each Domino stage consists of a dynamic inverter followed by a static inverter. Assume that the precharge
Chapter 6 Problem Set

time, evaluate time, and propagation delay of the static inverter are all \( T/2 \). Assume that the transitions are ideal (zero rise/fall times).

a. Complete the timing diagram for signals \( \text{Out}_1 \), \( \text{Out}_2 \), \( \text{Out}_3 \) and \( \text{Out}_4 \), when the \( \text{IN} \) signal goes high before the rising edge of the clock \( \phi \). Assume that the clock period is 10 \( T \) time units.

Solution

The timing diagram is shown below.

![Timing Diagram](image)

b. Suppose that there are no evaluate switches at the 3 latter stages. Assume that the clock \( \phi \) is initially in the precharge state (\( \phi=0 \) with all nodes settled to the correct precharge states), and the block enters the evaluate period (\( \phi=1 \)). Is there a problem during the evaluate period, or is there a benefit? Explain.

Solution

There is no problem during the evaluate stage. The precharged nodes remain charged until a signal propagates through the logic, activating the pull-down network and discharging the node. In fact, this topology improves the circuit’s robustness in terms of charge sharing affecting the output for any generic pull-down network, and reduces the body effect in the pull-down network.

c. Assume that the clock \( \phi \) is initially in the evaluate state (\( \phi=1 \)), and the block enters the precharge state (\( \phi=0 \)). Is there a problem, or is there any benefit, if the last three evaluate switches are removed? Explain.

Solution

There is a problem during the precharge stage. If all precharged nodes are discharged during the evaluate stage, when the precharge FETs simultaneously turn on, the pull-down

Figure 6.17 Conventional DOMINO Dynamic Logic.
networks will initially remain on, creating a short circuit. This continues in each gate until the previous gate charges, disabling its pull-down network.

24. [C. Spice, 4.3] Figure 6.18 shows a dynamic CMOS circuit in Domino logic. In determining source and drain areas and perimeters, you may use the following approximations: $AD = AS = W \times 0.625 \mu m$ and $PD = PS = W + 1.25 \mu m$. Assume 0.1 ns rise/fall times for all inputs, including the clock. Furthermore, you may assume that all the inputs and their complements are available, and that all inputs change during the precharge phase of the clock cycle.

a. What Boolean functions are implemented at outputs $F$ and $G$? If $A$ and $B$ are interpreted as two-bit binary words, $A = A_1 A_0$ and $B = B_1 B_0$, then what interpretation can be applied to output $G$?

**Solution**

$$F = A_0 B_0 + \overline{A}_1 \overline{B}_1, \quad G = F(A_0 B_0 + \overline{A}_1 \overline{B}_1)$$

If $A$ and $B$ are interpreted as two-bit binary words, output $G$ is high if $A = B$: a comparator.

b. Which gate (1 or 2) has the highest potential for harmful charge sharing and why? What sequence of inputs (spanning two clock cycles) results in the worst-case charge-sharing scenario? Using SPICE, determine the extent to which charge sharing affects the circuit for this worst case.

**Solution**

Gate 2 has the higher potential for harmful charge sharing because the capacitance that contributes to charge sharing is larger than in gate 1.

The sequence of inputs resulting in the worst-case charge sharing is $A_0 = B_0$ and $A_1 = B_1$ for the first cycle. Then $A_0 = B_0$ and $A_1 \neq B_1$ for the second cycle such that $A_j/A_j$ transistor that is on during the second cycle is the same as in the first cycle. For example, $A_0 = B_0 = A_j = B_j = V_{DD}$ in cycle 1 and $A_0 = B_0 = A_j = V_{DD}, B_j = 0$ V in cycle 2. This
will cause the charge at the output of gate 2 to be shared with the total parasitic capacitance at the drains of the $A_1$, $\overline{A}_1$, and $B_1$ transistors.

25. [M, Spice, 4.3] In this problem you will consider methods for eliminating charge sharing in the circuit of Figure 6.18. You will then determine the performance of the resulting circuit.

a. In problem 24 you determined which gate (1 or 2) suffers the most from charge sharing. Add a single 2/0.25 PMOS precharge transistor (with its gate driven by the clock $\phi$ and its source connected to $V_{DD}$) to one of the nodes in that gate to maximally reduce the charge-sharing effect. What effect (if any) will this addition have on the gate delay? Use SPICE to demonstrate that the additional transistor has eliminated charge sharing for the previously determined worst-case sequence of inputs.

Solution

The additional precharge transistor should charge the node that is shared by the $A_1$ and $\overline{A}_1$ transistor drains and the $F$ transistor source. Assuming the gate delay is dominated by the precharge stage, this will reduce the gate delay by briefly aiding the precharging of gate 2. SPICE output with additional precharge transistor.
b. For the new circuit (including additional precharge transistor), find the sequence of inputs (spanning two clock cycles) that results in the worst-case delay through the circuit. Remember that precharging is another factor that limits the maximum clocking frequency of the circuit, so your input sequence should address the worst-case precharging delay.

Solution
The worst-case delay results from \( A = B \) for two consecutive cycles. This results in the maximum charging and discharging of the internal nodes.

c. Using SPICE on the new circuit and applying the sequence of inputs found in part (b), find the maximum clock frequency for correct operation of the circuit. Remember that the precharge cycle must be long enough to allow all precharged nodes to reach \(~90\%\) of their final values before evaluation begins. Also, recall that the inputs (\( A, B \) and their complements) should not begin changing until the clock signal has reached 0 V (precharge phase), and they should reach their final values before the circuit enters the evaluation phase.

Solution
The maximum clock frequency is \(~4.4\) GHz.

26. [C, None, 4.2–3] For this problem, refer to the layout of Figure 6.19.

a. Draw the schematic corresponding to the layout. Include transistor sizes.

Solution
![Schematic Diagram]
b. What logic function does the circuit implement? To which logic family does the circuit belong?

**Solution**

The circuit implements \( \text{Out} = \overline{A} + BC \). It is in the pseudo NMOS family.

c. Does the circuit have any advantages over fully complementary CMOS?

**Solution**

The circuit uses less area than a fully complementary CMOS implementation.

d. Calculate the worst-case \( V_{OL} \) and \( V_{OH} \).

**Solution**

\[ V_{OH} = V_{DD} = 2.5V. \] To find \( V_{OL} \), assume that we can combine \( M_B \) and \( M_C \) into one NMOS with \( W/L = 0.75/0.25 \). Then the worst case \( V_{OL} \) occurs when \( A = 0 \) and the combined BC NMOS is on. Assume that \( V_{OL} \) is less than \( V_{DSAT} \). Then the NMOS device is in the linear region. The PMOS device will be velocity saturated. Equating the currents at the output gives:

\[ k_p \cdot \frac{W}{L} \cdot V_{DSAT} \cdot (V_{GT} - 0.5V_{DSAT}) \cdot (1 + \lambda V_{DS}) + k_n \cdot \frac{W}{L} \cdot V_o \cdot (V_{GT} - 0.5V_o) \cdot (1 + \lambda V_o) = 0 \]

The only unknown in this 3rd order polynomial is \( V_o \). Solving for \( V_o \) gives \( V_{OL} = 51.2mV \)

e. Write the expressions for the area and perimeter of the drain and source for all of the FETs in terms of \( \lambda \). Assume that the capacitance of shared diffusions divides evenly between the sharing devices. Copy the layout into Magic, extract and simulate to find the worst-case \( t_{pHL} \) time. For what input transition(s) does this occur? Name all of the parasitic capacitances that you would need to know to calculate this delay by hand (you do not need to perform the calculation).

**Solution**

Call the PMOS device \( P \), and name the other devices by their input signal.

\[ AD_P = AS_P = 19\lambda^2, \quad PD_P = PS_P = 15\lambda. \]
\[ AS_A = 40\lambda^2, \quad PS_A = 18\lambda. \]
\[ AD_A = (3x8 + 3x12) \lambda^2 / 2 = 30 \lambda^2 \cdot PD_A = 16 \lambda / 2 = 8 \lambda. \]
\[ AD_B = AD_A, PD_B = PD_A. \]
\[ AS_B = 36 \lambda^2 / 2 = 18 \lambda^2 \cdot PS_B = 6 \lambda / 2 = 3 \lambda. \]
\[ AD_C = AS_B, PD_C = PS_C. \]
\[ AS_C = 60 \lambda^2, PS_C = 22 \lambda. \]

We can narrow the number of transitions to look at for determining the worst case \( t_{\text{HL}}. \)
The worst case capacitance occurs when the internal node between \( M_B \) and \( M_C \) is charged up to \( V_{DD} \). Then the worst case delay will occur when either \( M_A \) or the \( M_B, M_C \) pair discharges this capacitance. If the series devices are doing the discharging, we need to consider the case where \( M_B \) is initially on and where \( M_B \) is initially off.

The simulation shows that the worst-case transition occurs over three cycles: ABC = 010 to 000 to 011 produces the worst-case \( t_{\text{HL}} \). This is worse than when \( MA \) discharges the node (ABC = 010 to 110) or when \( MB \) is initially on (ABC = 010 to 011).

We could calculate \( t_{\text{HL}} \) using either the equivalent resistance method or the average current method. In either case, \( C_L \) would include the following parasitic capacitances:
\[ C_{GDPMOS} + C_{DBPMOS} + C_{GDA} \text{(no Miller effect b/c input not changing)} + C_{DBA} + C_{GDB} + C_{DBB} + C_{GB} + C_{GDC} + C_{DBC}. \]

27. **[E, None, 4.4]** Derive the truth table, state transition graph, and output transition probabilities for a three-input XOR gate with independent, identically distributed, uniform white-noise inputs.

**Solution**

The truth table of a three-input XOR gate is:

<table>
<thead>
<tr>
<th>A</th>
<th>B</th>
<th>C</th>
<th>Y</th>
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</thead>
<tbody>
<tr>
<td>0</td>
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</tbody>
</table>

Table 1: Truth table

As the inputs are independent, identically distribute, uniform white noise, each of the possible combinations of three input values, has a probability equal to 1/8. From the table, the probability of having the output equal to 0 is \( p_0 = 0.5 \). In the same way

28. **[C, None, 4.4]** Figure 6.20 shows a two-input multiplexer. For this problem, assume independent, identically-distributed uniform white noise inputs.

a. Does this schematic contain reconvergent fan-out? Explain your answer.

**Solution**
This schematic has reconvergent fan-out because both inputs of the or gate depend on the value of S.

b. Find the exact signal \((P_1)\) and transition \((P_{0 \rightarrow 1})\) formulas for nodes X, Y, and Z for: (1) a static, fully complementary CMOS implementation, and (2) a dynamic CMOS implementation.

**Solution**

Assuming a fully complementary CMOS implementation:

X is the output of an AND gate with independent, identically-distributed uniform white noise inputs. As only when both inputs are equal to 1 the output is 1, \(P_1 = 0.25\). On the other hand, \(P_{0 \rightarrow 1} = P_0 P_1 = 0.25(1 - 0.25) = 0.1875\).

Y is also the output of an AND gate with independent, identically distributed uniform white noise inputs. The analysis is the same as with X.

If we represent the truth table of the schematic we will see that \(P_1 = 0.5\). Then \(P_{0 \rightarrow 1} = P_0 P_1 = 0.5(1 - 0.5) = 0.25\).

Assuming a dynamic CMOS implementation:

In the same way as before, for X, \(P_1 = 0.25\). In order to obtain the transition probability, an n-tree dynamic gate will be assumed. In this case: \(P_{0 \rightarrow 1} = P_0 = 0.75\).

The analysis for Y is equal to the analysis for X.

For Z, using the truth table of the schematic we obtain, again, \(P_1 = 0.5\). For the transition probability, it will be assumed that a np-CMOS structure is used. Then, Z is the output of a p-tree dynamic gate. Then: \(P_{0 \rightarrow 1} = P_1 = 0.5\).

29. [M, None, 4.4] Compute the switching power consumed by the multiplexer of Figure 6.20, assuming that all significant capacitances have been lumped into the three capacitors shown in the figure, where \(C = 0.3\) pF. Assume that \(V_{DD} = 2.5\) V and independent, identically-distributed uniform white noise inputs, with events occurring at a frequency of 100 MHz. Perform this calculation for the following:

a. A static, fully-complementary CMOS implementation

**Solution**

Switching power is:

\[ P_{SW} = \alpha \cdot f \cdot C \cdot V_{DD}^2 = (\alpha_{X \rightarrow 1} + \alpha_{Y \rightarrow 1} + \alpha_{Z \rightarrow 1}) \cdot f \cdot C \cdot V_{DD}^2 \]

We calculated in Problem 27 the probabilities of a 0->1 transition for each node:

\(P_{0 \rightarrow 1}\) for X and Y is 0.1875 and \(P_{0 \rightarrow 1}\) for Z is 0.25.

Thus, \(P_{SW} = (2^2 \cdot 0.1875 + 0.25) \cdot 100\text{MHz} \cdot 0.3\text{pF} \cdot 2.5^2 = 117.2\text{uW}\).

b. A dynamic CMOS implementation

**Solution**
In Problem 27 for a dynamic np-CMOS gate, we calculated the probabilities: \( P_{X \to 1} = 0.75 \) and \( P_{Z \to 1} = 0.5 \). Thus, \( P_{SW} = (2 \times 0.75 + 0.5) \times 100MHz \times 0.3pF \times 2.5^2 = 375uW \).

30. For the circuit shown Figure 6.21 ignore DIBL and \( S=100mV/\text{decade} \).

a. What is the logic function implemented by this circuit? Assume that all devices (M1-M6) are 0.5\( \mu \)m/0.25\( \mu \)m.

Solution
\[ A(B+C) \]

b. Let the drain current for each device (NMOS and PMOS) be 1\( \mu \)A for NMOS at \( V_{GS} = V_T \) and PMOS at \( V_{SG} = V_T \). What input vectors cause the worst case leakage power for each output value? Explain (state all the vectors, but do not evaluate the leakage).

Solution
When the output is high, the worst-case leakage occurs when two transistors leak in parallel: \( ABC = 100 \). When the output is low, the worst-case leakage also occurs when two transistors leak in parallel: \( ABC = 110 \) or \( ABC = 101 \).

c. Suppose the circuit is active for a fraction of time \( d \) and idle for \((1-d)\). When the circuit is active, the inputs arrive at 100 MHz and are uniformly distributed (\( Pr(A = 1) = 0.5 \), \( Pr(B = 1) = 0.5 \), \( Pr(C = 1) = 0.5 \)) independent. When the circuit is in the idle mode, the inputs are fixed to one you chose in part (b). What is the duty cycle \( d \) for which the active power is equal to the leakage power?

\[ d*P_{\text{active}} = (1-d)P_{\text{leakage}} \]

\[ P_{\text{active}} = \alpha_{0 \to 1} f^2 C_L \frac{V_{DD}^2}{V_T^2} = (3/8 \times 5/8)(100 \times 10^6)^2(50 \times 10^{-15})^2(2.5)^2 = 7.3 \mu W \]

\[ P_{\text{leakage}} (ABC = 100) = V_{DD} \times 2 * I_{\text{leakM1}} = 5 \times 10^{-10} \times 5 = 5 \times 1 \mu A 10^{-10} = 251pW \]

Plugging the power numbers into the activity equation and solving for \( d \) gives \( d = 3.4 \times 10^{-6} \).
**DESIGN PROJECT**

Design, lay out, and simulate a CMOS four-input XOR gate in the standard 0.25 micron CMOS process. You can choose any logic circuit style, and you are free to choose how many stages of logic to use; you could use one large logic gate or a combination of smaller logic gates. The supply voltage is set at 2.5 V! Your circuit must drive an external 20 fF load in addition to whatever internal parasitics are present in your circuit.

The primary design objective is to minimize the propagation delay of the worst-case transition for your circuit. The secondary objective is to minimize the area of the layout. At the very worst, your design must have a propagation delay of no more than 0.5 ns and occupy an area of no more than 500 square microns, but the faster and smaller your circuit, the better. Be aware that, when using dynamic logic, the precharge time should be made part of the delay.

The design will be graded on the magnitude of $A \times t_p^2$, the product of the area of your design and the square of the delay for the worst-case transition.